

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

Inventor(s): Hitoshi IRINO
DOCKET NO.: 045054-0158

FIG. 1

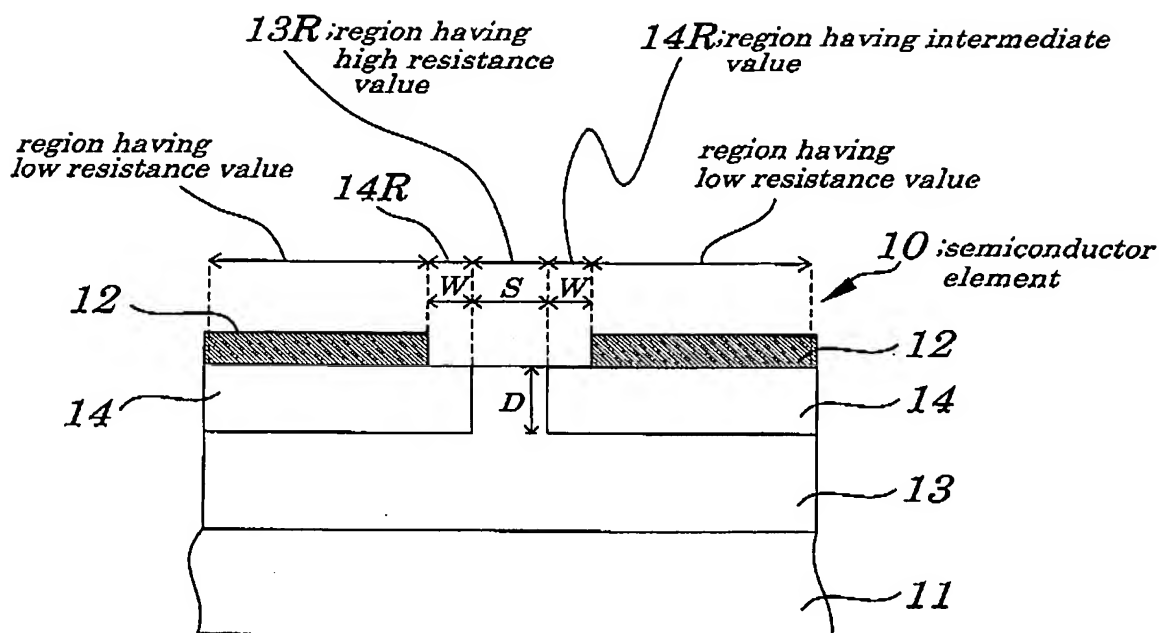


FIG. 2

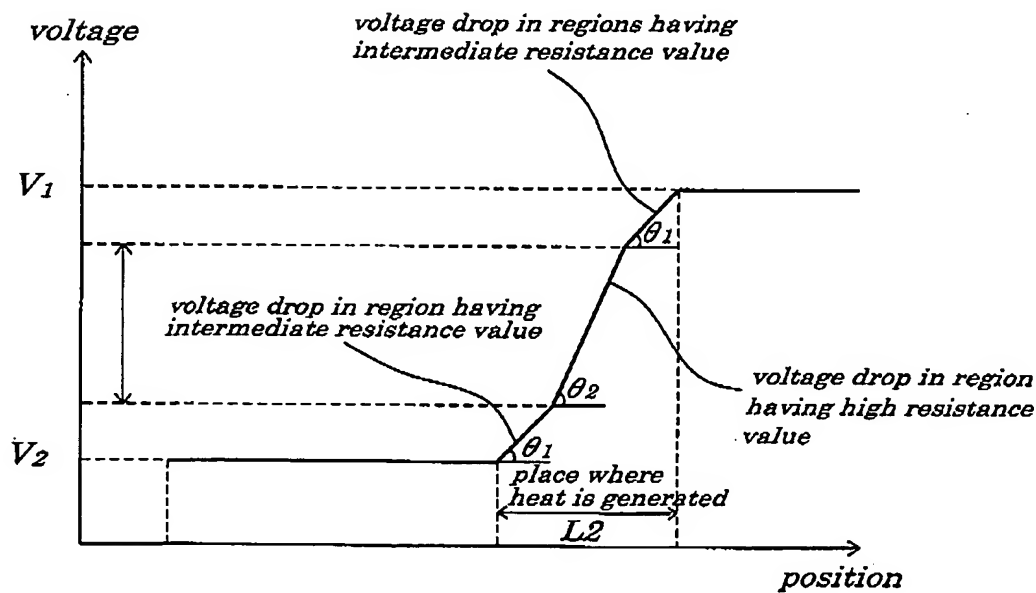


FIG. 3A (PRIOR ART)

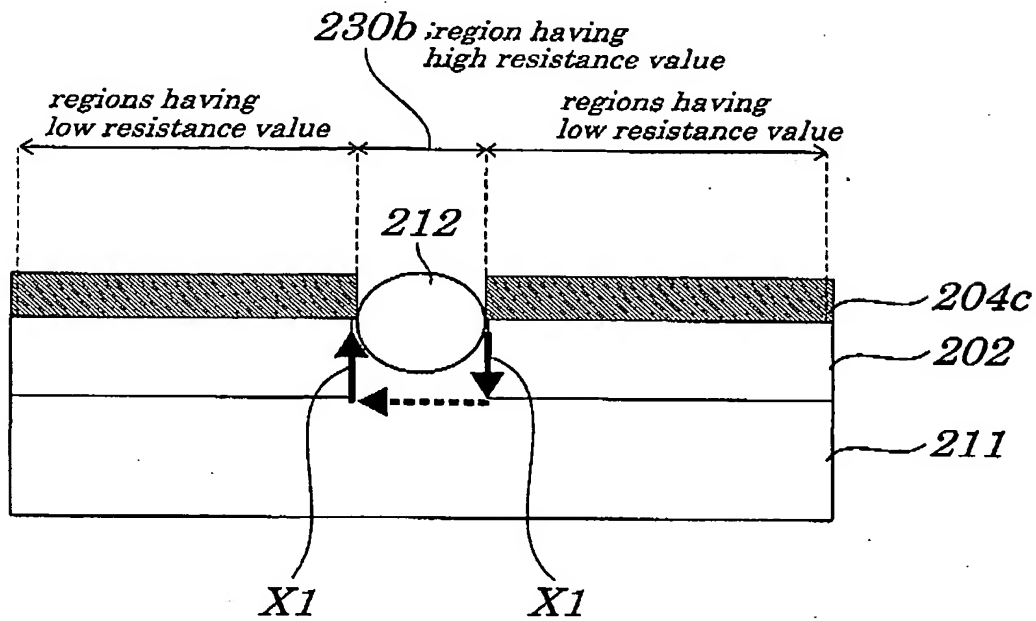


FIG. 3B

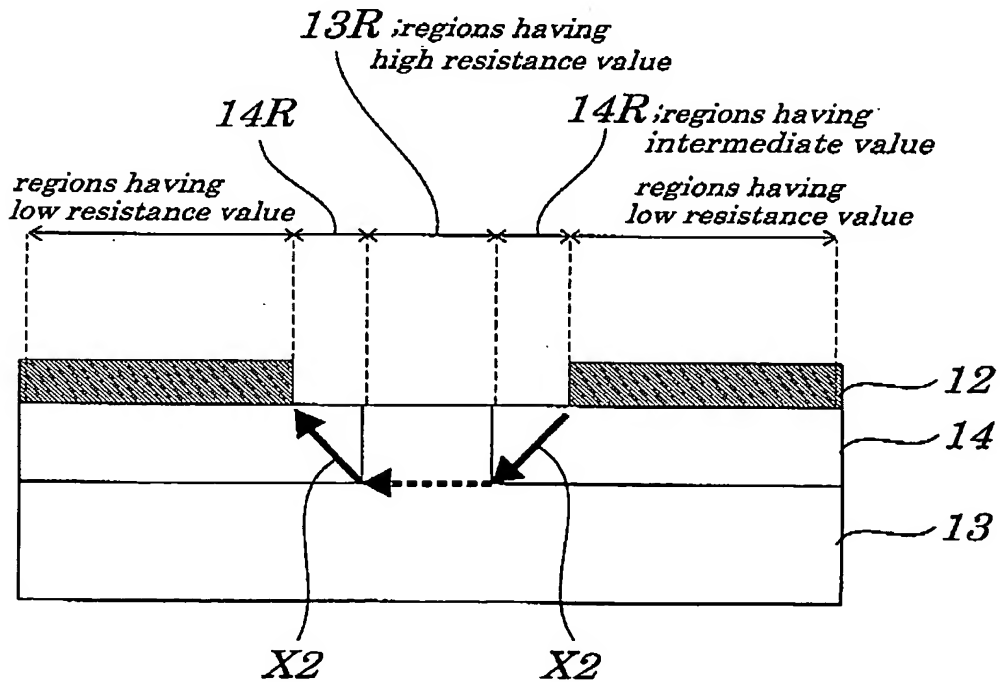


FIG. 4A

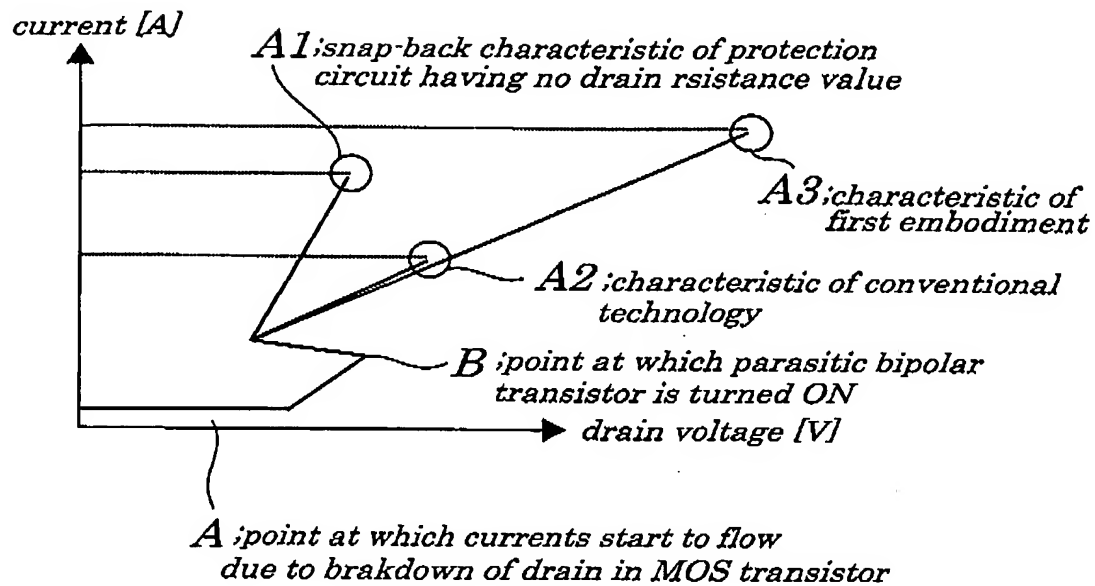


FIG. 4B

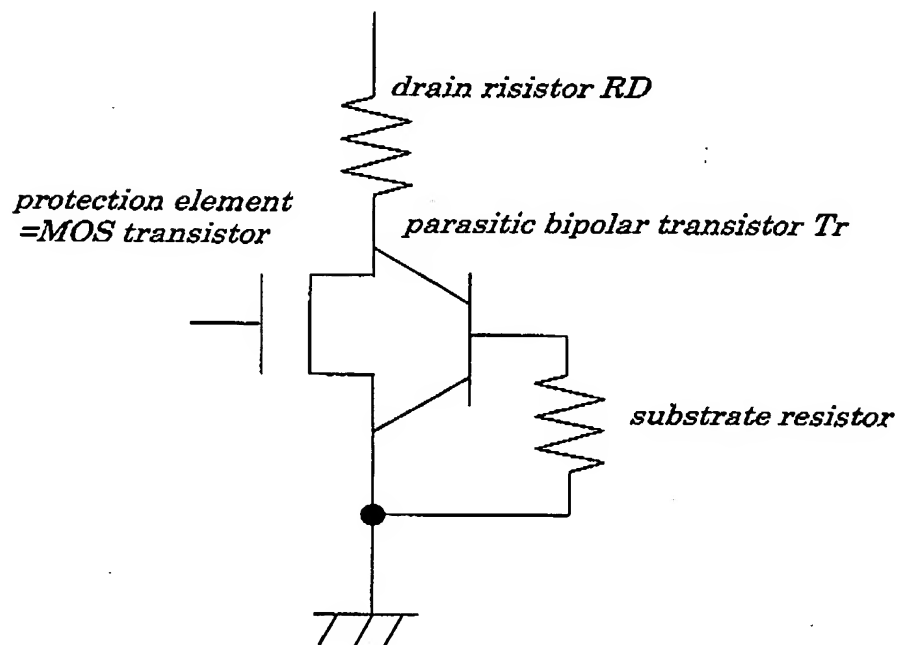


FIG.5

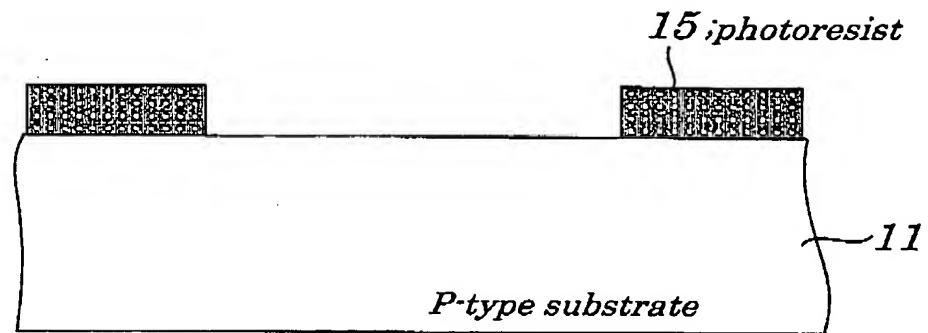


FIG.6

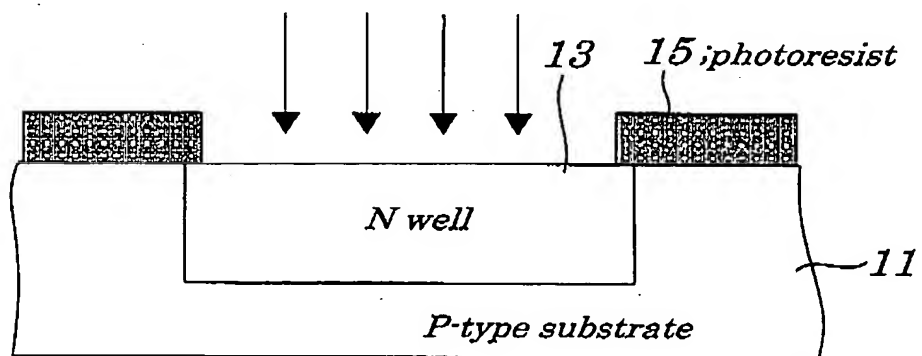


FIG. 7

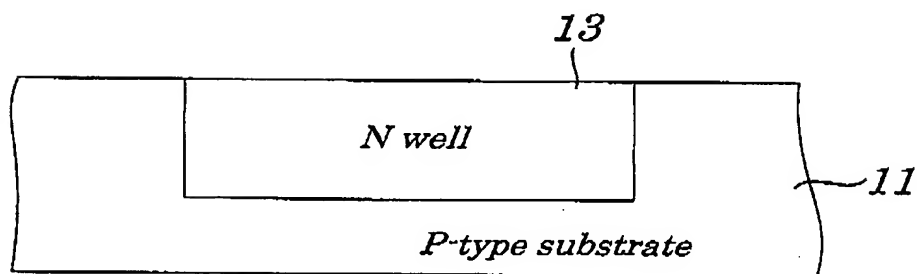


FIG. 8

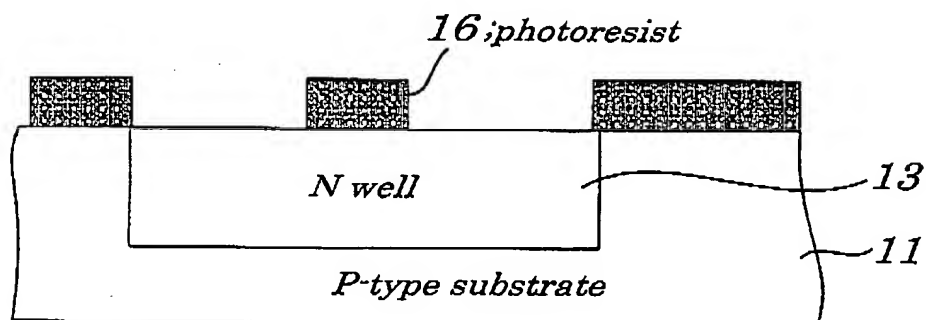


FIG. 9

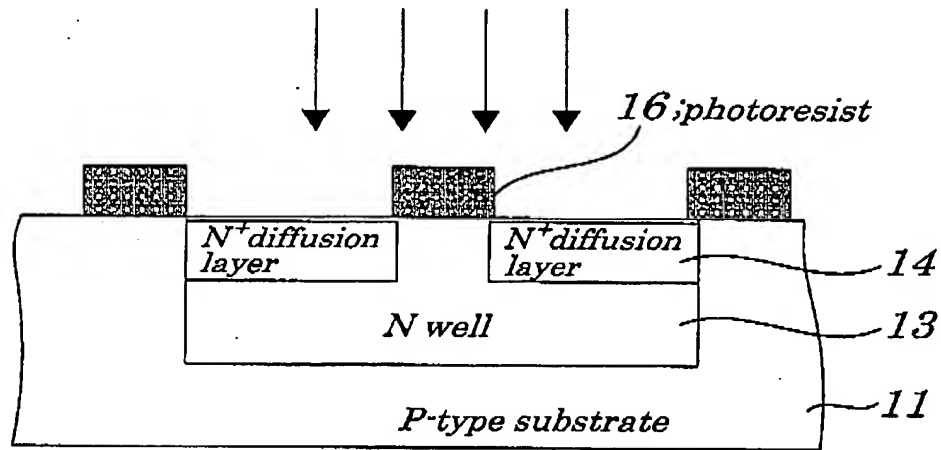


FIG. 10

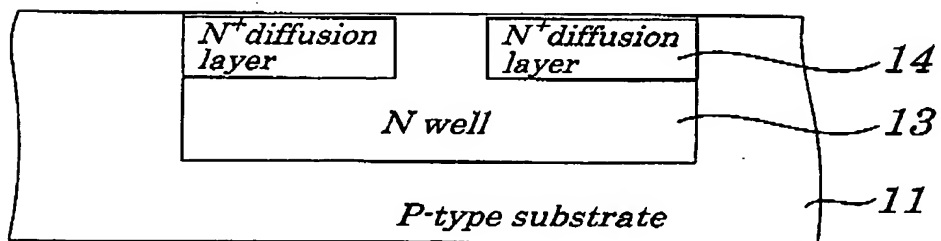


FIG.11

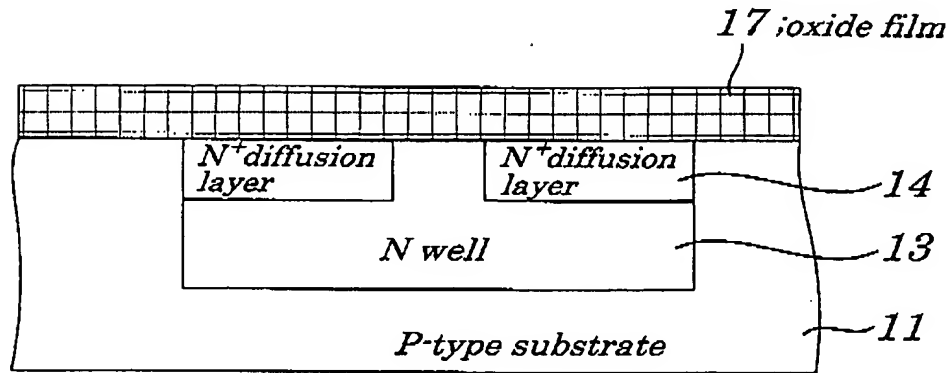


FIG.12

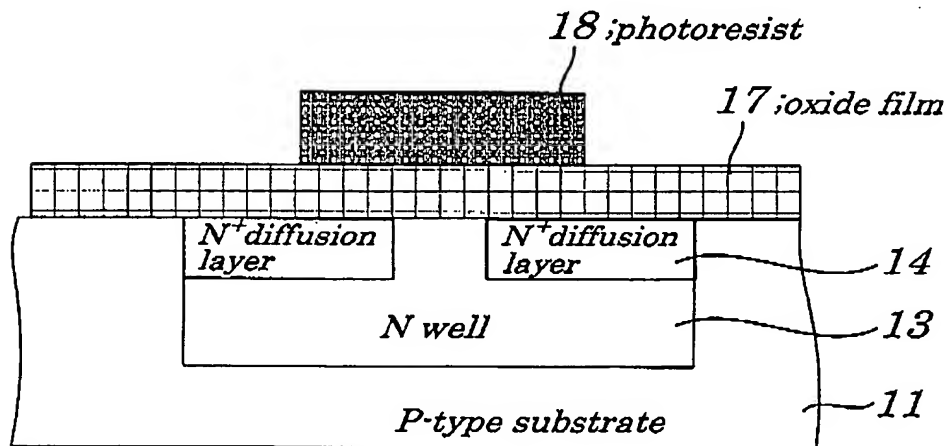


FIG.13

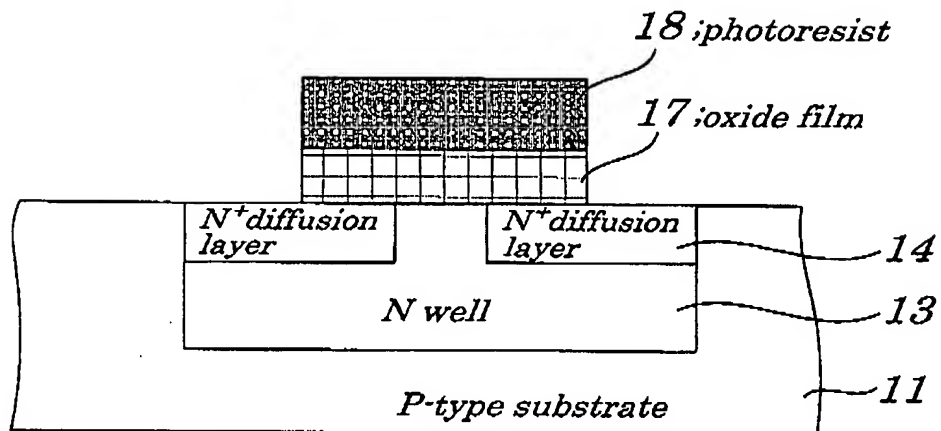


FIG.14

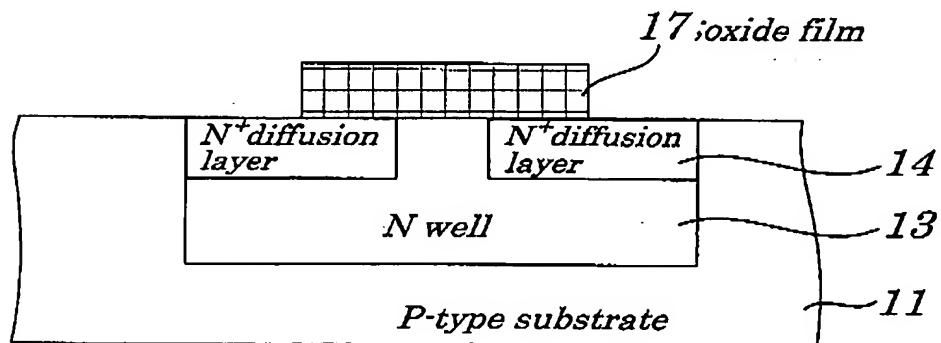


FIG.15

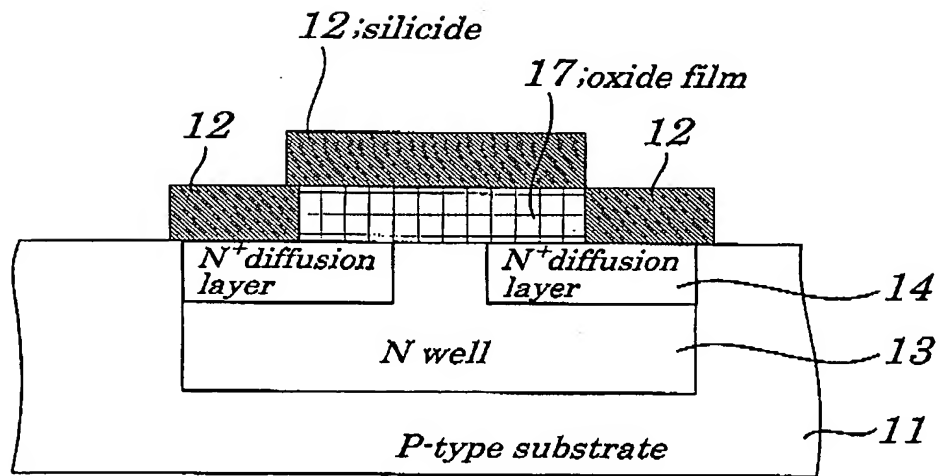


FIG.16

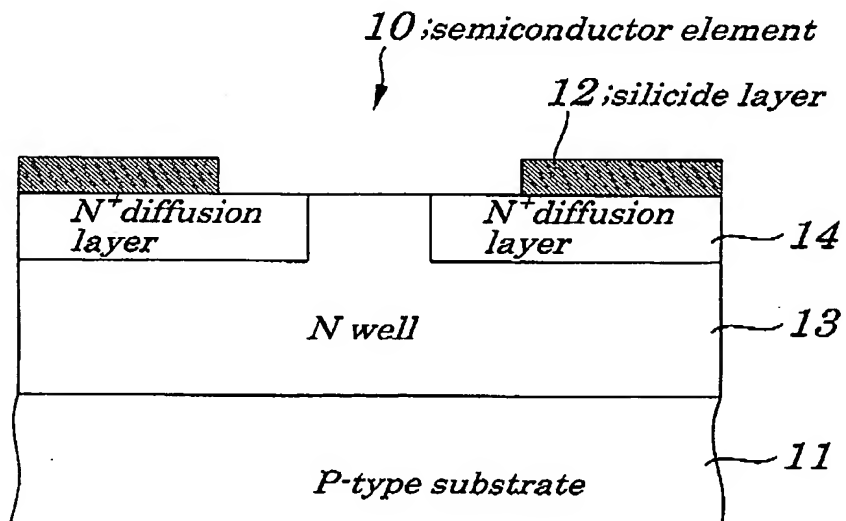


FIG.17

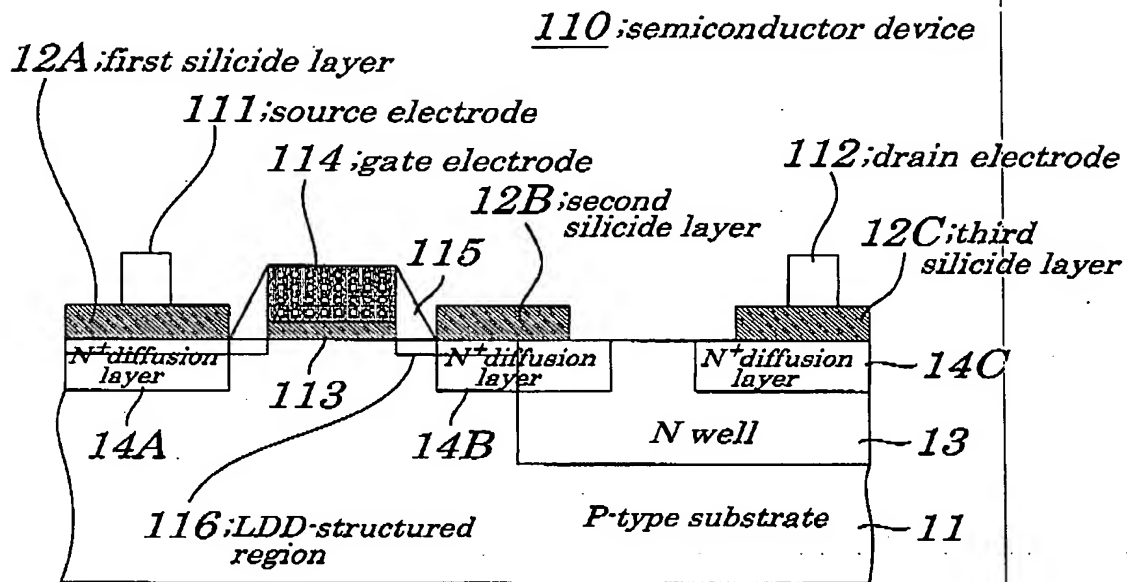


FIG.18

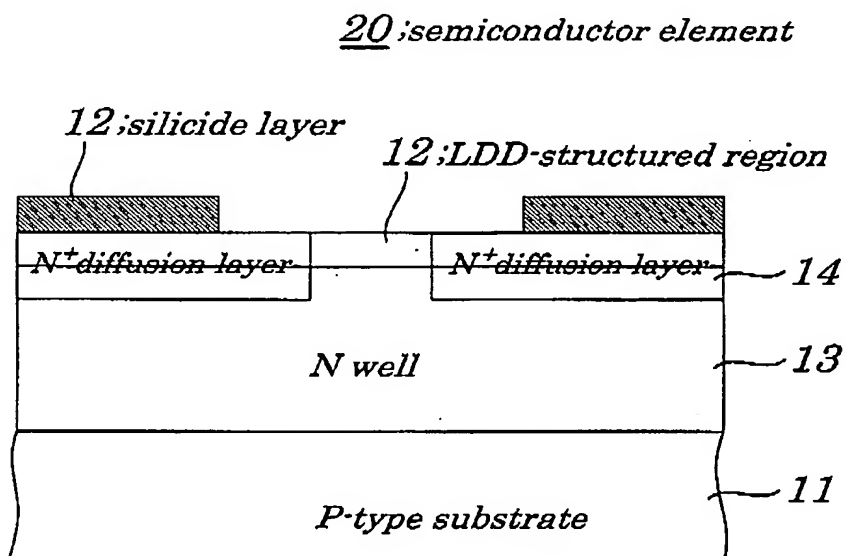


FIG.19

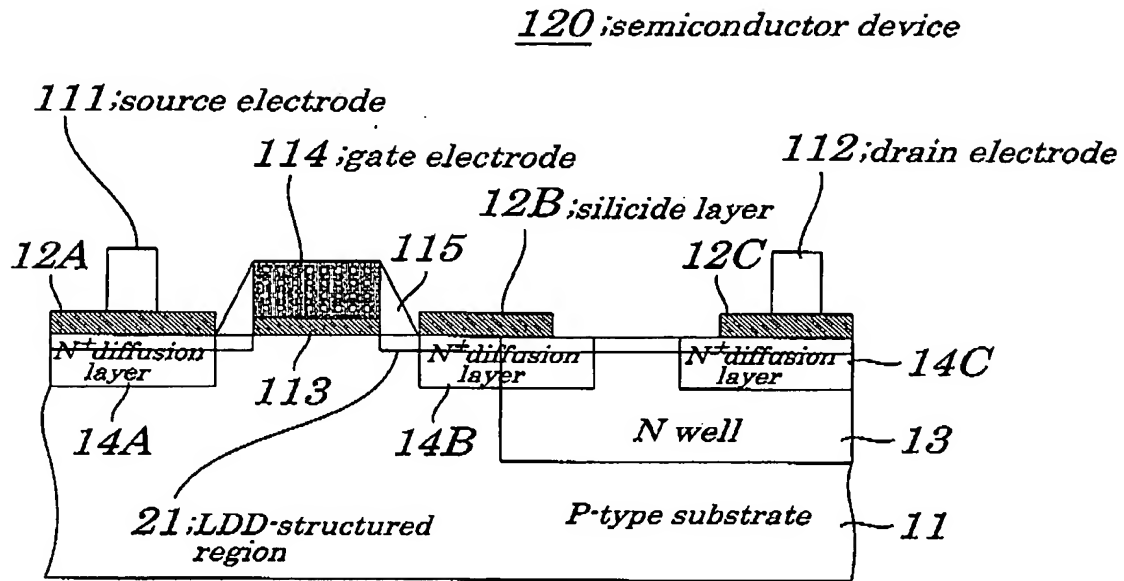


FIG.20

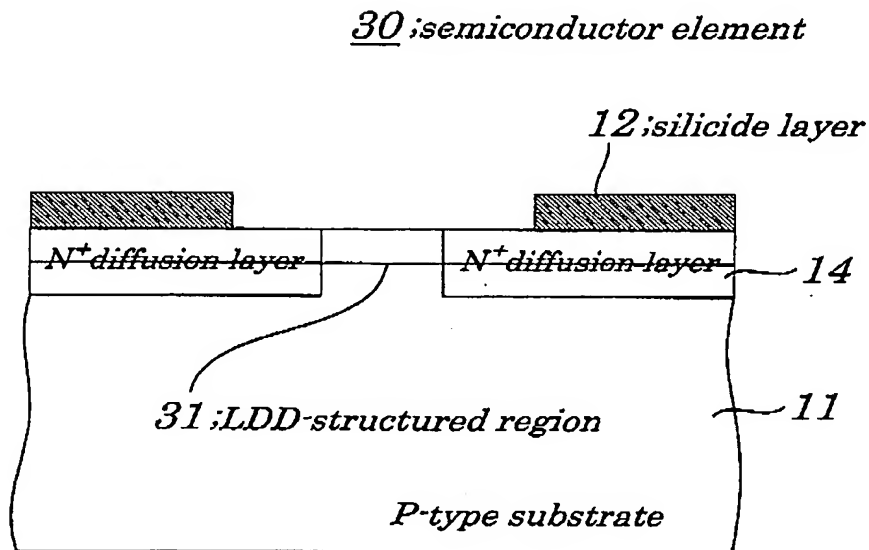


FIG.21

130; semiconductor device

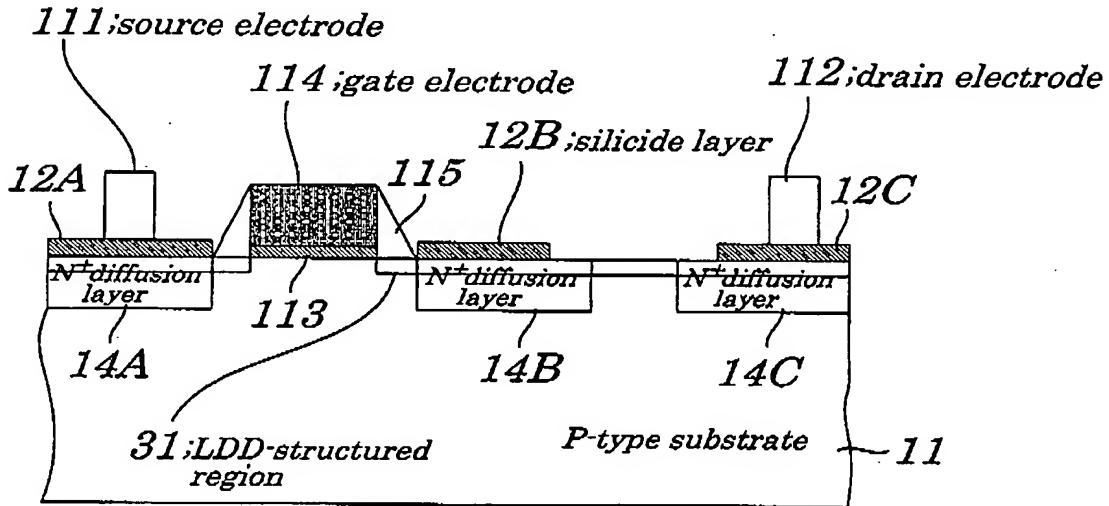


FIG.22

40; semiconductor element

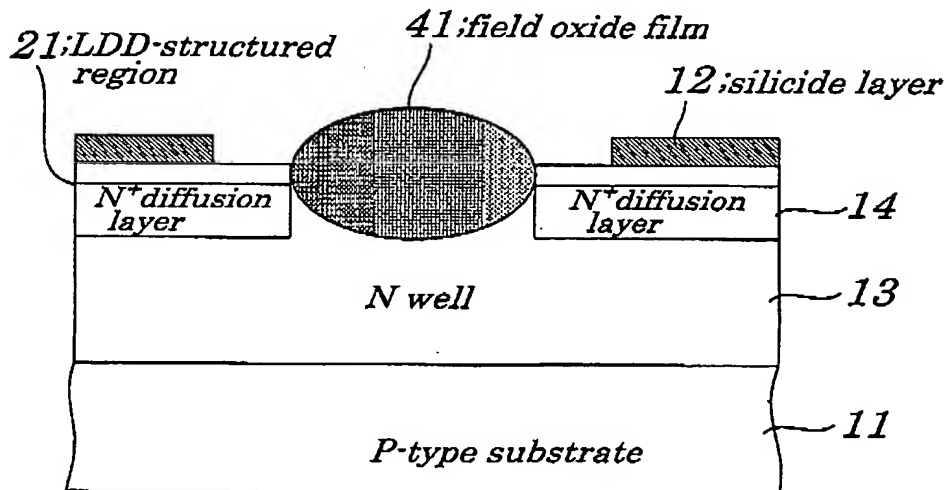


FIG.23

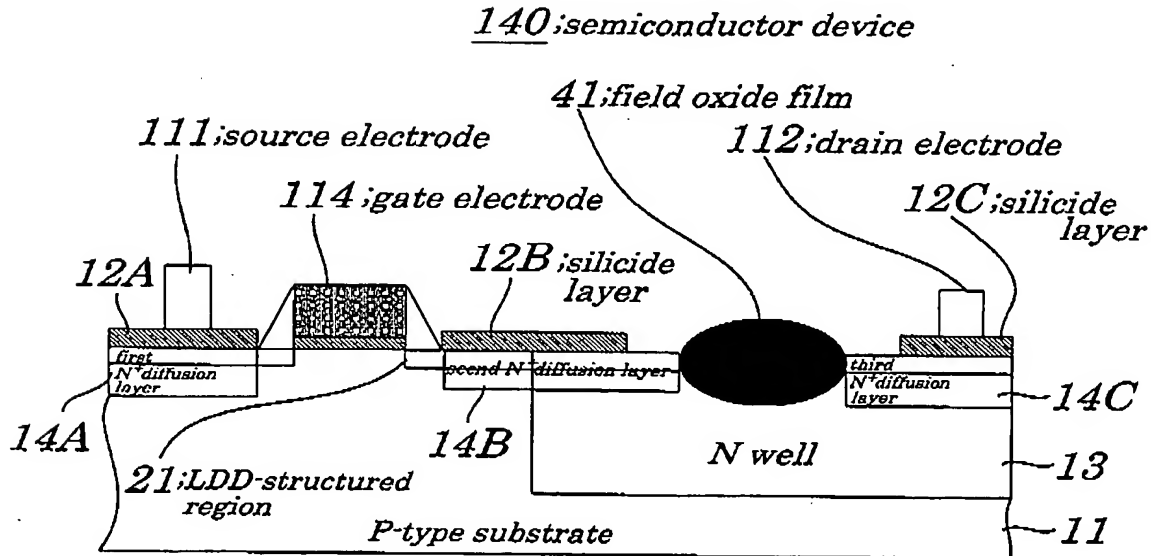


FIG.24

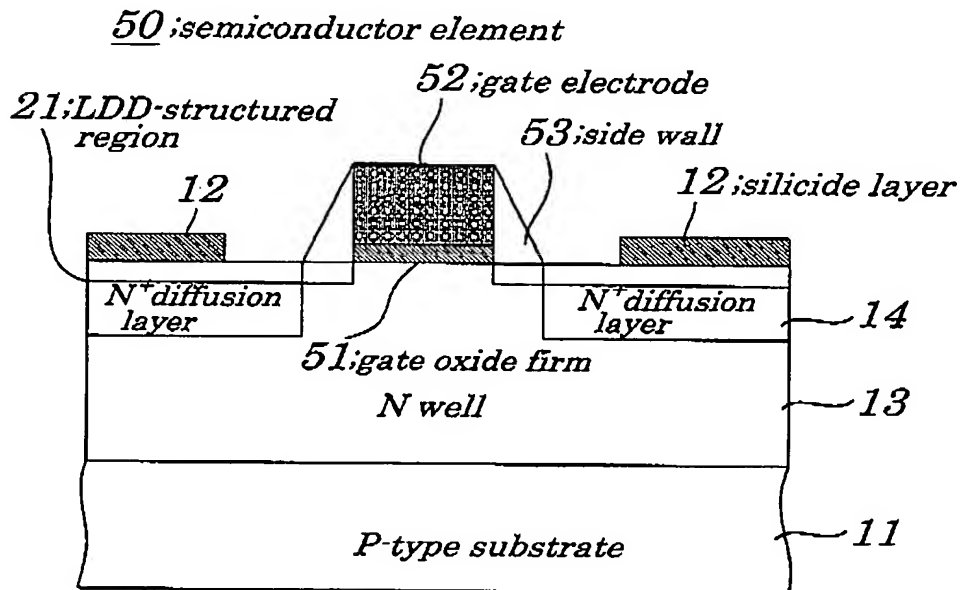


FIG.25

150;semiconductor device

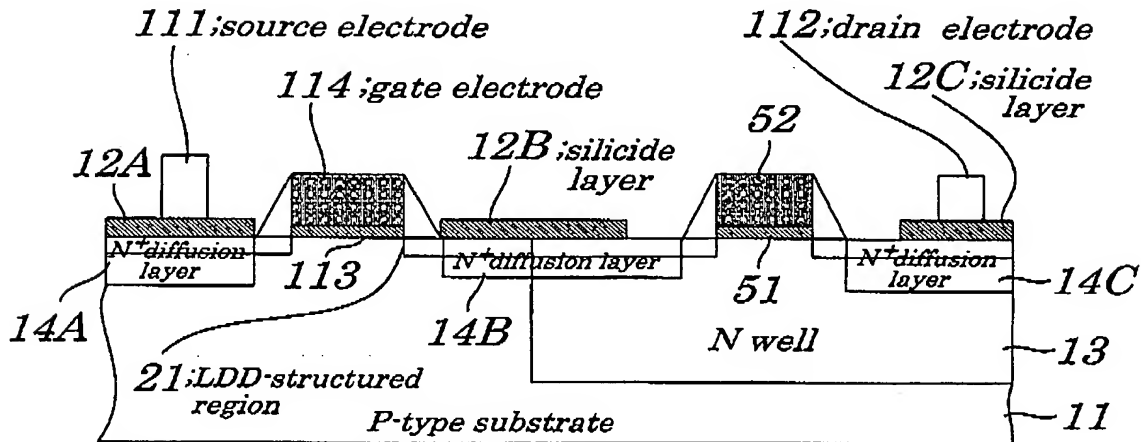


FIG.26 (PRIOR ART)

200;semiconductor device

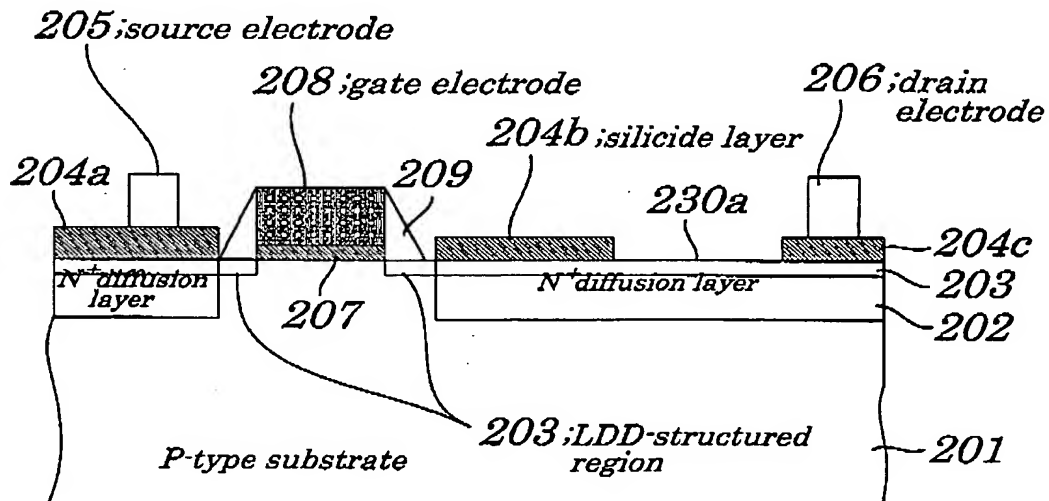


FIG.27 (PRIOR ART)

210;semiconductor device

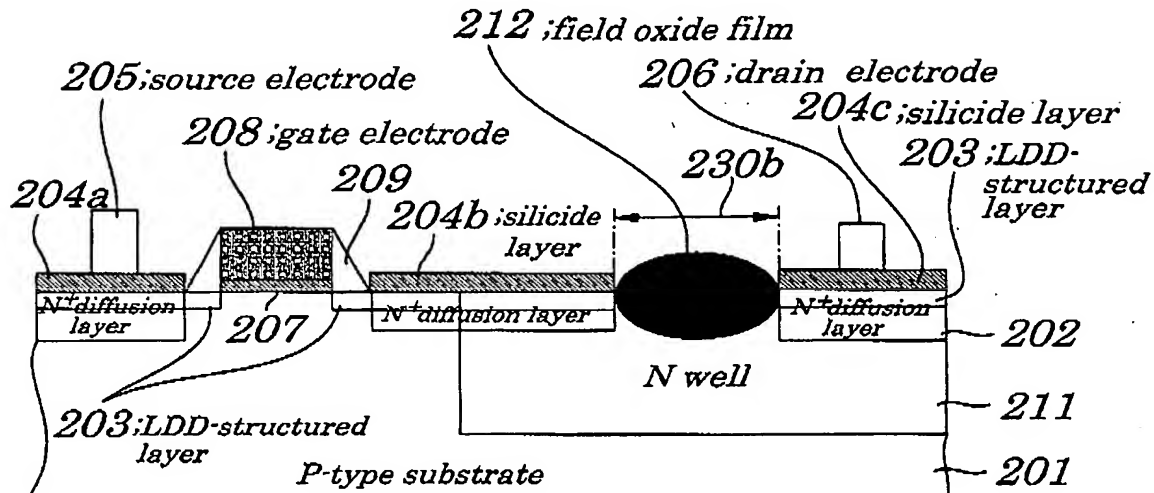


FIG.28 (PRIOR ART)

220;semiconductor device

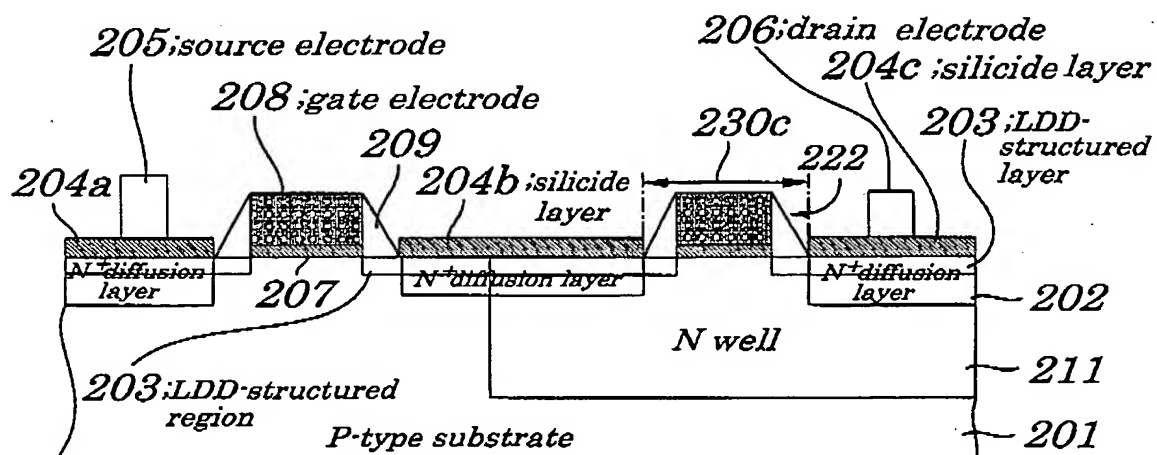


FIG. 29A (PRIOR ART)

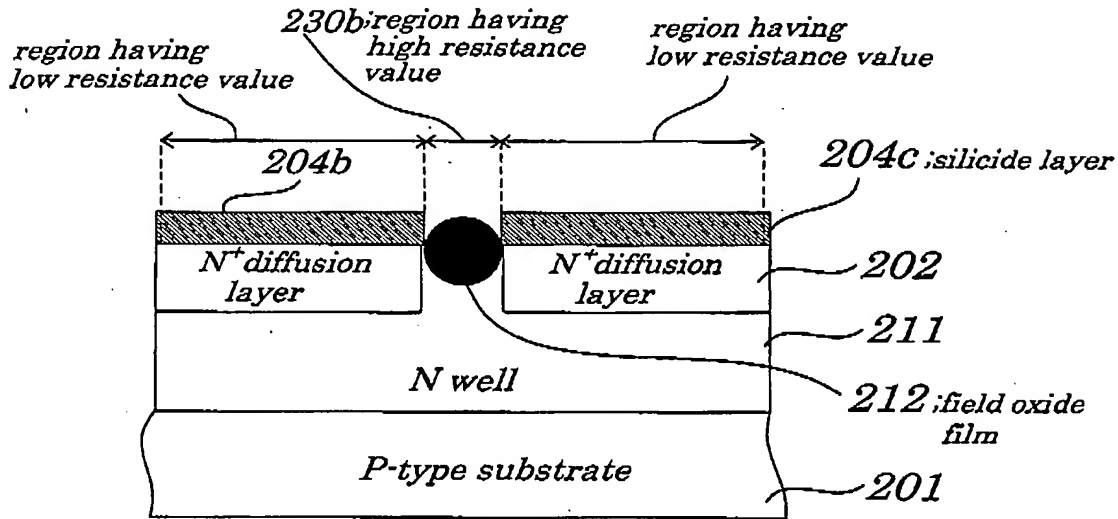


FIG. 29B (PRIOR ART)

